

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:
a semiconductor substrate; and
a first magneto resistive element separated from
5 said semiconductor substrate, said first magneto
resistive element comprising a first magnetic layer and
a first nonmagnetic layer, said first magnetic layer
and said first nonmagnetic layer being formed in
a direction perpendicular to said semiconductor
10 substrate.

2. A semiconductor memory device according to
claim 1, wherein said first magneto resistive element
continues over a plurality of cells.

3. A semiconductor memory device according to
15 claim 1, wherein said first magneto resistive element
is divided in units of cells.

4. A semiconductor memory device according to
claim 1, further comprising:

first wiring which is separated from said
20 semiconductor substrate and extends in a first
direction; and

second wiring which is separated from said first
wiring and extends in a second direction different from
the first direction, said first magneto resistive
25 element being separated from said first and second
wiring.

5. A semiconductor memory device according to

claim 4, wherein said first magneto resistive element continues over a plurality of cells.

5 6. A semiconductor memory device according to claim 4, wherein said first magneto resistive element is divided in units of cells.

 7. A semiconductor memory device according to claim 4, further comprising third wiring which is separated from said second wiring, extends in the second direction, and is connected to said first
10 magneto resistive element.

 8. A semiconductor memory device according to claim 1, further comprising:

 first wiring which is separated from said semiconductor substrate and extends in a first
15 direction;

 second wiring which is separated from said first wiring and extends in a second direction different from the first direction; and

 fourth wiring which is formed away from said second wiring with a first space therebetween, is
20 separated from said first wiring, and extends in the second direction, said first magneto resistive element being formed in the first space away from said first, second, and fourth wiring.

25 9. A semiconductor memory device according to claim 8, wherein said first magneto resistive element continues over a plurality of cells.

10. A semiconductor memory device according to claim 8, wherein said first magneto resistive element is divided in units of cells.

5 11. A semiconductor memory device according to claim 8, further comprising third wiring which is separated from said second wiring, extends in the second direction, and is connected to said first magneto resistive element.

10 12. A semiconductor memory device according to claim 1, further comprising:

first wiring which is separated from said semiconductor substrate and extends in a first direction;

15 second wiring which is separated from said first wiring and extends in a second direction different from the first direction;

20 fourth wiring which is formed away from said second wiring with a first space therebetween, is separated from said first wiring, and extends in the second direction, said first magneto resistive element being formed in the first space away from said first, second, and fourth wiring; and

25 a second magneto resistive element which is formed in the first space away from said first, second, and fourth wiring and from said first magneto resistive element, and comprising a second magnetic layer and a second nonmagnetic layer, said second magnetic layer

and said second nonmagnetic layer being formed in a direction perpendicular to said semiconductor substrate.

13. A semiconductor memory device according to
5 claim 12, wherein said first and second magneto resistive elements continue over a plurality of cells.

14. A semiconductor memory device according to claim 12, wherein said first and second magneto resistive elements are divided in units of cells.

10 15. A semiconductor memory device according to claim 12, wherein a first stacked structure comprising said first magnetic layer and said first nonmagnetic layer and a second stacked structure comprising said second magnetic layer and said second nonmagnetic layer
15 are axially symmetrical with respect to the boundary between said first and second magneto resistive elements.

16. A semiconductor memory device according to claim 12, further comprising third wiring which is
20 separated from said second wiring, extends in the second direction, and is connected to said first magneto resistive element.

17. A semiconductor memory device according to claim 12, further comprising a contact formed between
25 said first and second magneto resistive elements to connect said first and second magneto resistive elements to said first wiring.

18. A semiconductor memory device according to claim 17, wherein at least said first and second magneto resistive elements or said contact continues over a plurality of cells.

5 19. A semiconductor memory device according to claim 17, wherein at least said first and second magneto resistive elements or said contact is divided in units of cells.

10 20. A semiconductor memory device according to claim 1, further comprising:

first wiring which is separated from said semiconductor substrate and extends in a first direction;

15 second wiring which is formed above and away from said first wiring, and extends in a second direction different from the first direction;

20 fourth wiring which is formed away from said second wiring with a first space therebetween, is formed above and away from said first wiring, and extends in the second direction, said first magneto resistive element being formed in the first space away from said first, second, and fourth wiring;

25 a second magneto resistive element which is formed in the first space away from said first, second, and fourth wiring and from said first magneto resistive element, is formed above said first wiring, and comprising a second magnetic layer and a second

nonmagnetic layer, said second magnetic layer and said second nonmagnetic layer being formed in a direction perpendicular to said semiconductor substrate; and

5 fifth wiring which is formed away from said fourth wiring with a second space narrower than the first space therebetween, is formed above and away from said first wiring, and extends in the second direction.

21. A semiconductor memory device according to claim 20, wherein said first and second magneto
10 resistive elements continue over a plurality of cells.

22. A semiconductor memory device according to claim 20, wherein said first and second magneto resistive elements are divided in units of cells.

23. A semiconductor memory device according to claim 20, further comprising third wiring which is
15 separated from said second wiring, extends in the second direction, and is connected to said first magneto resistive element.

24. A semiconductor memory device according to claim 20, wherein a first stacked structure comprising
20 said first magnetic layer and said first nonmagnetic layer and a second stacked structure comprising said second magnetic layer and said second nonmagnetic layer are axially symmetrical with respect to the boundary
25 between said first and second magneto resistive elements.

25. A semiconductor memory device according to

claim 20, further comprising a contact formed between said first and second magneto resistive elements to connect said first and second magneto resistive elements to said first wiring.

5 26. A semiconductor memory device according to claim 25, wherein at least said first and second magneto resistive elements or said contact continues over a plurality of cells.

10 27. A semiconductor memory device according to claim 25, wherein at least said first and second magneto resistive elements or said contact is divided in units of cells.

15 28. A semiconductor memory device according to claim 20, wherein the first and second spaces alternately exist on the same level.

 29. A semiconductor memory device according to claim 1, wherein said first magneto resistive element is a TMR element in which said first nonmagnetic layer is a tunnel junction layer.

20 30. A semiconductor memory device according to claim 1, wherein

 said first magneto resistive element is a TMR element in which said first nonmagnetic layer is a tunnel junction layer, and

25 said TMR element comprises a single tunnel junction structure including one tunnel junction layer, or a double tunnel junction structure including

two tunnel junction layers.

31. A method of manufacturing a semiconductor memory device, comprising:

5 forming first wiring above a semiconductor substrate;

 forming a first insulating film on the first wiring;

 forming second and fourth wiring on the first insulting film, the fourth wiring being formed away
10 from the second wiring with a first space therebetween;

 partially forming a second insulating film on the first insulating film and on the second and fourth wiring to form a first trench in the first space;

 forming first and second magneto resistive
15 elements on two side surfaces of the first trench, the first magneto resistive element comprising a first magnetic layer and a first nonmagnetic layer, the first magnetic layer and the first nonmagnetic layer being formed in a direction perpendicular to the
20 semiconductor substrate, the second magneto resistive element comprising a second magnetic layer and a second nonmagnetic layer, and the second magnetic layer and the second nonmagnetic layer being formed in the direction perpendicular to the semiconductor substrate;

25 removing the first insulating film from a bottom surface of the first trench between the first and second magneto resistive elements to form a contact

hole which exposes a portion of the first wiring, and removing a portion of the second insulating film which are positioned above the second and fourth wiring to form second and third trenches;

5 forming a contact in the contact hole, the contact being connected to the first wiring and to the first and second magneto resistive elements; and

 forming third and sixth wiring in the second and third trenches, respectively, the third wiring being
10 connected to the first magneto resistive element, and the sixth wiring being connected to the second magneto resistive element.

32. A method according to claim 31, wherein the formation of the first and second magneto resistive
15 elements comprises:

 forming a magnetic layer material on the bottom surface and two side surfaces of the first trench and on the second insulating film;

 removing the magnetic layer material on the bottom
20 surface of the first trench and on the second insulating film to form the first and second magnetic layers on the two side surfaces of the first trench;

 forming a nonmagnetic layer material on the bottom surface of the first trench, on the side surfaces of
25 the first and second magnetic layers, and on the second insulating film; and

 removing the nonmagnetic layer material on

the bottom surface of the first trench and on the second insulating film to from the first and second nonmagnetic layers on the side surfaces of the first and second magnetic layers.

5 33. A method of manufacturing a semiconductor memory device according to claim 31, wherein at least the first and second magnetic resistive elements or the contact is divided in units of cells.

10 34. A method of manufacturing a semiconductor memory device according to claim 31, further comprising forming the third and sixth wiring into predetermined shapes, and at the same time dividing at least the first and second magneto resistive elements or the contact in units of cells.

15 35. A method of manufacturing a semiconductor memory device according to claim 31, further comprising forming fifth wiring away from the second or fourth wiring with a second space narrower than the first space therebetween, simultaneously with the formation
20 of the second and fourth wiring.

 36. A method of manufacturing a semiconductor memory device according to claim 35, further comprising forming seventh and eighth wiring simultaneously with the formation of the second, fourth, and fifth wiring,
25 the seventh wiring being formed away from the fifth wiring with the first space therebetween, and the eighth wiring being formed away from the seventh wiring

with the second space therebetween.

37. A method of manufacturing a semiconductor
memory device according to claim 35, wherein the first
and second magneto resistive elements are TMR elements
5 in which the first and second nonmagnetic layers are
tunnel junction layers.